Total No. of Printed Pages:2

SUBJECT CODE :82
FACULTY OF ENGINEERING AND TECHNOLOGY
S.E. (EC/ECT/IEC/E&C) Examination Nov/Dec 2015
Digital Logic Design
(Revised)

[Time: Three Hours] **[Max. Marks: 80]**

"Please check whether you have got the right question paper."

N.B i) Q.No.1 and Q.No.6 are compulsory.
ii) Attempt any two questions from the remaining questions in each section.
iii) A figure to the right indicates full marks
iv) Assume suitable data wherever necessary.

Section-A

Q1. Solve any five from the following 10

i. Explain DTCL
ii. What is the use of don't care condition
iii. Explain half substractor
iv. What are the Bipolar logic families
v. Convert 0011 into gray
vi. What is multiplexer, List out the types.
vii. Compare SOP & POS
viii. What is Active pull up in TTL logic

Q.2 a) Design binary to gray code converter 08

b) Explain TTL logic in detail 07

Q.3 a) Simplify logic function using K-MAP $f(A, B, C)=\pi_m(0,1,3,5) + d\ (4,6)$ 07

b) Simplify logic function using Quine-Mcclusky technique $f(A,B,C,D)=\sum_m(0,1,3,4,7,9,10,13,15)$ 08

Q.4 a) Design 32:1 multiplexer using 16:1 multiplexer 08

b) Compare CMOS & TTL 07

Q.5 Write short note on (any three) 15

i. Parallel adder 7483
ii. Magnitude comparator
iii. ALU
iv. PAL
v. HDL

Section-B

Q.6 Solve any five from the following 10

i. State the application of Flip Flop
ii. How T Flip Flop operator?
iii. Explain static RAM

iv. Explain truth table of S-R Flip Flop
v. Define propagation delay
vi. Explain flash memory
vii. State the advantages of successive approximation A/D converter
viii. Explain the concept Dual slope A/D converter

Q.7 a) Explain Master slave J-K Flip Flop 08

b) Explain SISO & PIPO with diagram 07

Q.8 a) Explain ring counter in detail 07

b) Design mode 10 counter 08

Q.9 a) Compare RAM &ROM & classify the memory 07

b) Draw and explain 4 bit Up-Down counter 08

Q.10 Write short note on the following (Any three) 15

i. Flip Flop conversion
ii. Classification and characteristics and memory
iii. Sequence generation and detection
iv. How to design Asynchronous counter
v. Johnson's counter

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