

FACULTY OF ENGINEERING
S.E.(EC/ECT/IE/E&C)Examination - DEC - 2014
Digital Logic Design(Revised)

[Time: THREE Hours]

[Max. Marks: 80]

“Please check whether you have got the right question paper.”

- N.B**
- i) Question no. s 1&6 are compulsory.
 - ii) Attempt any two questions from the remaining, in each section.
 - iii) A figure to the right indicates full marks.
 - iv) Assume suitable data wherever necessary.

SECTION A

- | | | |
|-----|--|---------------------|
| Q.1 | Solve any five from the following: | 10 |
| | <ol style="list-style-type: none"> i) Define and explain ‘Noise margin’. ii) Comment on ‘Don’t care conditions’. iii) Compare Demultiplexer and decoder iv) Using the conversion method, carry out the conversion of T to JK. v) What is race around condition? vi) What is Tri –state Logic? Explain. vii) Explain the need of BCD to seven segment decoder. viii) What is the use of karnaugh map? | |
| Q.2 | <ol style="list-style-type: none"> a) Design a Binary to Gray code converter. b) Design 32:1 multiplexer using 8:1 multiplexers. | <p>08</p> <p>07</p> |
| Q.3 | <ol style="list-style-type: none"> a) Explain the operation of a two input CMOS NAND gate. b) State the advantages and disadvantages of ECL logic family over other logic families. | <p>08</p> <p>07</p> |
| Q.4 | <ol style="list-style-type: none"> a) Draw K-map for the following function simplify and realize it by using NAND gates only.
 $f = ABC\bar{D} + \bar{B}\bar{C} + \bar{B}D + ABC\bar{D} + \bar{B}C$ b) Design a full –subtractor using NAND gates only. | <p>08</p> <p>07</p> |
| Q.5 | Write short notes on the following :- | 15 |
| | <ol style="list-style-type: none"> i) PAL ii) Min term and max term iii) DCTL iv) Quine –Mc Clusky technique v) ALU | |

SECTION B

Q.6	Solve any five from the following :-	10
	i) State the applications of flip-flops.	
	ii) Explain how the up or down counting selection is done.	
	iii) How does D flip-flop operate?	
	iv) Compare static RAM and dynamic RAM.	
	v) Differentiate between synchronous counter and asynchronous counter.	
	vi) What is preset and clear terminal in a flip-flop? Why these terminals are active low?	
	vii) Write a note on cascading of Demultiplexers.	
	viii) State the advantages of successive approximation A/D converter.	
Q.7	a) Draw and explain the clocked S-R flip-flop and its working .Also explain its truth table.	07
	b) Carry out the following conversions –	08
	i)JK to D	
	ii) SR to T	
Q.8	a) Design a 4-bit synchronous counter counting from 0 to 15. specify the IC required.	08
	b) How will you use the shift register to multiply or divide a binary number? Explain	07
Q.9	a) Explain in detail the memory classification used in digital Electronics	08
	b) Explain Moore machines	07
Q.10	Write short notes on the following (any three)	15
	i) Sequential logic circuits	
	ii) Johnson counter	
	iii) PROM	
	iv) Digital Comparator	
	v) D to A convertors	