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**CODE NO:- Z-352**

**FACULTY OF ENGINEERING & TECHNOLOGY**  
**S.E(EC/ECT/ IEC/E&C)Year Examination June – 2015**  
**Digital Logic Design**  
**(Revised)**

[Time: Three Hours]

[Max. Marks: 80]

“Please check whether you have got the right question paper.”

- i) Question no.1 & 6 are compulsory
- ii) Attempt any two questions from the remaining in each section.
- iii) Figures to the right indicate full marks.
- iv) Assume suitable data, Wherever necessary

**SECTION A**

- Q.1 Solve any five from the following : 10
- a) Define and explain ‘Fan in’.
  - b) Comment on Tri- state logic.
  - c) Explain important features of Gray code.
  - d) Convert the gray code ‘1011’ to binary
  - e) Compare ECL and CMOS families.
  - f) What is the difference between encoder and multiplexer.
  - g) Clearly state the use of parity generators and checkers
  - h) Write a note on HDL.
- Q.2 a) Design a 7:128 decoder using 4=16 decoder. 08  
b) Design a BCD to 7-segment decode using gates 07
- Q.3 a) Explain the following characteristics of digital logic families: 08
- i) Speed logic operation
  - ii) Power dissipation
  - iii) Noise immunity
  - iv) Current and voltage parameters
- b) Explain in detail the TTL family. 07
- Q.4 a) Minimize the four variable logic function with the use of K-map : 08  
 $f(A,B,C,D) = \pi M(4,6,10,12,13,15)$
- b) What is De-multiplexer? Explain the need of De-mux in digital electronics, what are the different ICs used for Mux and Demux. 07
- Q.5 Write short notes on the following(any three) : 15
- a) Digital comparator IC7485.
  - b) Karnaugh map representation
  - c) NMOS logic family
  - d) Read only memory
  - e) Half –sub tractors

## SECTION-B

- Q.6 Solve any five from the following : 10
- a) Draw the circuit for 4 bit R-2R D/A converter?
  - b) Explain the concept 'Dual slope A/D conversion'.
  - c) What is race around condition in J-K F/F?
  - d) What is the difference between RAM & ROM?
  - e) Explain the concepts of King counter.
  - f) What is a D-type latch?
  - g) Distinguish between synchronous and asynchronous counter
  - h) Explain the use of preset and clear terminals in a flip –flop
- Q.7 a) Give the design procedure for asynchronous counter. 08  
b) Draw and explain the working of universal shift register. 07
- Q.8 a) Design a 4 bit up counter using J-K flip –flops. 08  
b) Explain sequence generation and detection. 07
- Q.9 a) With the help of suitable diagram explain the successive approximation method of A/D conversion .Also state its advantages. 10  
b) Compare EPROM with EEPROM. 05
- Q.10 Write short notes on the following (any three) 15
- a) Flip-flop conversion
  - b) mealy machines
  - c) State diagram and state table
  - d) Classification and characteristics of memories
  - e) SRAM and DRAM.