

SUBJECT CODE:- 302
FACULTY OF ENGINEERING AND TECHNOLOGY
B.E.(EC/ECT/E&C/IE) Examination Nov/Dec 2015
VLSI Design
(Revised)

[Time: Three Hours]

[Max. Marks: 80]

“Please check whether you have got the right question paper.”

- N.B
- i) Question no .1 & question No. 6 are compulsory.
 - ii) Solve any two questions from Q. no. 2 to Q. no 5.
 - iii) Solve any two questions from Q. no 7 to Q .no 10.
 - iv) Figures to the right indicate full marks.
 - v) Assume suitable data if necessary.

Section A

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|-----|---|----------|
| Q.1 | Attempt any two from the following | 10 |
| | <ol style="list-style-type: none"> a) State and explain Moore’s Law. b) Compare verilog with VHDL. c) What is testability? Explain the need of design for testability. d) What is mean by synthesizable and non-synthesizable statements? | |
| Q.2 | <ol style="list-style-type: none"> a) Explain the various types of architecture modeling styles used in VHDL with example. b) Explain different classes of data object in VHDL with example. | 08
07 |
| Q.3 | <ol style="list-style-type: none"> a) Explain attributes and configuration in VHDL. b) Write the VHDL code for 4 bit UP counter. | 08
07 |
| Q.4 | <ol style="list-style-type: none"> a) Explain types of fault and fault coverage. b) Explain TAP controller with state diagram. | 08
07 |
| Q.5 | <ol style="list-style-type: none"> a) State the features of FPGA. Explain architecture of FPGA. b) Write the VHDL code for <ol style="list-style-type: none"> i) 1:8 DEMUX ii) J-K flip-flop. | 07
08 |

Section- B

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|------|--|----------|
| Q.6 | Attempt any two from the following | 10 |
| | <ol style="list-style-type: none"> a) Explain the operation of N-MOS transistor. b) Explain transmission gate with example. c) Explain Body effect in CMOS. d) Explain the terms noise margin and power delay product? | |
| Q.7 | <ol style="list-style-type: none"> a) What is CMOS inverter? Explain its DC transfer characteristics: b) Design CMOS logic for $Y = \overline{(W + xv)}(Z + U)$ | 08
07 |
| Q.8 | <ol style="list-style-type: none"> a) Explain CMOS logic families. b) Explain pass transistor logic with example. | 08
07 |
| Q.9 | <ol style="list-style-type: none"> a) Explain p-well CMOS fabrication process in detail. b) Explain the layout – design rules in CMOS processing technology. | 08
07 |
| Q.10 | <ol style="list-style-type: none"> a) Explain in detail static and dynamic power dissipation. What are the components which makes power dissipation in CMOS circuit. b) Explain in detail analysis of CMOS inverter with parasitic. | 08
07 |

