Total No. of Printed Pages:2

SUBJECT CODE NO:- P-110
FACULTY OF ENGINEERING AND TECHNOLOGY
B.E.(EC/ECT/E&C/IE) Examination MAY/JUNE-2016
VLSI Design
(Revised)

[Time:Three Hours] **[Max Marks:80]**

"Please check whether you have got the right question paper."

N.B
i) Question No.1 and Question No.6 are compulsory.
ii) Solve any two questions from Q.No.2 to Q.No.5.
iii) Solve any two questions from Q.No.7 to Q.No.10.
iv) Figures to the right indicate full marks.
v)Assume suitable data, if necessary and state it clearly.

Section A

Q.1 Attempt any two from the following. 10
a) Compare VHDL and verilog.
b) Write the short note on EDA tools.
c) Compare FPGA and CPLD family.
d) Describe JTAG technology.

Q.2 a) Explain VLSI Design flow. 07
b) Write the VHDL code for 16:1 MUX using 8:1 MUX. 08

Q.3 a) Explain concept of package and library. 07
b) Explain architecture of XC4000 FDGA family. 08

Q.4 a) With suitable example, explain operation of TAP controller. 08
b) Explain boundary scan testing in detail. 07

Q.5 a) What is component declaration and component instantiation? Explain with example. 07
b) Explain different classes of data object in VHDL with example. 08

Section B

Q.6 Attempt any two from the following. 10
a) What is body effect? How it affects on the threshold voltage?
b) Explain velocity saturation and mobility degradation in CMOS transistor.
c) Explain skewed gates in static CMOS transistor.
d) Explain design rules for CMOS technology.

Q.7 a) Explain why junction leakage and tunneling current is higher for NMOS than PMOS transistors. 07
b) Explain noise margin and power dissipation with respect to CMOS. 08

Q.8 a) Design CMOS logic gates for following functions. 08

i. $F_1 = \overline{AB + DE + C}$

ii. $F_2 = \overline{A + B + C + D}$

b) Explain pass transistor logic with suitable example. 07

Q.9 a) Explain twin-tub process for CMOS fabrication. 08

b) Explain layout of CMOS inverter. 07

Q.10 Write short notes on (Any three) 15

i. CMOS inverter with parasitic

ii. Body effect

iii. Transmission gate

iv. Bi CMOS inverter