[Total No. of Printed Pages:1] **CODE NO:- Z-64**

FACULTY OF ENGINEERING

B.E (ECT/EC/E&C/IE) Year Examination - May – 2015

VLSI Design

(Revised)

[Time: Three *Hours*] **[Max. Marks:80]**

"Please check whether you have got the right question paper."

i) Question No. 1 and Question No.6 are compulsory.
ii) Solve any two questions from Q. No.2 to Q. No.5
iii) Solve any two questions from Q. No.7 to Q. No.10
iv) Figures to the right – indicate full marks.
v) Assume suitable data if necessary & state it clearly

SECTION-A

Q.1 Attempt any two from the following 10

a) Explain integrated circuit technology
b) Write in brief on EDA tools
c) Compare FPGA and CPLD family.
d) Describe JTAG technology.

Q.2 a) Explain different language elements of VHDL. 07
b) Write the VHDL code for BCD to 7 segment decoder. 08

Q.3 a) Explain function and procedure in VHDL with example. 07
b) Explain architecture of XC9500 CPLD family 08

Q.4 a) Explain stuck at 1 and stuck at 0 faults. 07
b) Explain the term controllability obeservability and fault coverage. 08

Q.5 a) Write VHDL code for 4-bit comparator. 07
b) Write the VHDL code for 8-bit shift register 08

SECTION-B

Q.6 Attempt any two from the following 10

a) Draw and explain IV characteristics of NMOS transistor.
b) Explain velocity saturation & mobility degration in CMOS transistor.
c) Explain skewed gates in static CMOS transistor.
d) Explain self aligned process in CMOS.

Q.7 a) Explain subthreshold conduction current concept with its importance 07
b) Explain why junction leakage and tunneling current is higher for nMos than PMOS transistors. 08

Q.8 a) What are the types of CMOS logic families? Explain Ratio circuits. 08
b) Explain pass transistor logic with suitable example. 07

Q.9 a) Explain n-well CMOS fabrication process in detail. 07
b) State and explain the layout design rules in CMOS processing technology. 08

Q.10 Write short notes on (any three) 15

a) CLM
b) Body effect
c) Transmission gate
d) CMOS fabrication schemes